

CLAIMS

What is claimed is:

- 1 1. A method of manufacturing a double-gate integrated circuit comprising:
2 forming a laminated structure having a channel layer and first insulating
3 layers on each side of said channel layer;
4 forming openings in said laminated structure;
5 forming drain and source regions in said openings;
6 doping said drain and source regions, using said openings in said
7 laminated structure to align said doping;
8 removing portions of said laminated structure to leave said channel layer
9 suspended from said drain and source regions;
10 forming a second insulating layer to cover said drain and source regions
11 and said channel layer; and
12 forming a double-gate conductor over said second insulating layer such
13 that said double-gate conductor includes a first conductor on a first side of said
14 channel layer and a second conductor on a second side of said channel layer.

- 1 2. The method in claim 1, wherein, during said forming of said double-gate
2 conductor, said drain and source regions and said second insulating layer self-
3 align said double-gate conductor.

1 3. The method in claim 1, wherein said forming of said laminated structure
2 includes forming a bottom insulator layer adjacent one of said first insulating
3 layers and said method further comprises, after said forming of said double-gate
4 conductor, forming a top insulator layer on an opposite side of said double-gate
5 conductor from said bottom insulator layer, such that a thickness of said second
6 insulating layer is independent of a thickness of said bottom insulator layer and
7 said top insulator layer.

1 4. The method in claim 1, wherein said forming of said drain and source
2 regions comprises epitaxially growing drain and source regions in said openings
3 from said channel layer.

1 5. The method in claim 4, wherein said epitaxially growing of said drain and
2 source regions includes introducing one or more of Si, Ge, C, N and an alloy.

1 6. The method in claim 1, wherein said forming of said drain and source
2 regions comprises epitaxially growing a portion of said drain and source regions
3 in said openings from said channel layer and filling a remainder of said openings
4 with amorphous silicon to complete said drain and source regions.

1 7. The method in claim 1, wherein:

2 said forming of said laminated structure includes attaching a substrate to
3 said laminated structure;

4 said forming of said openings includes exposing said substrate; and
5 said forming of said drain and source regions comprises epitaxially
6 growing said drain and source regions in said openings from said channel layer
7 and said substrate.

1 8. The method in claim 1, wherein said channel layer comprises a single
2 crystal silicon layer and said forming of said laminated structure includes
3 depositing said first insulating layers on each side of said single crystal silicon
4 wafer.

1 9. The method in claim 1, wherein, before said forming of said drain and
2 source regions, said method further comprises forming spacers in said openings.

1 10. A method of manufacturing a double-gate metal oxide semiconductor
2 transistor comprising:

3 forming a laminated structure having a single crystal silicon channel layer
4 and insulating oxide and nitride layers on each side of said single crystal silicon
5 channel;

6 forming openings in said laminated structure;

7 forming drain and source regions in said openings;

8 doping said drain and source regions, using said openings in said
9 laminated structure to align said doping;
10 removing portions of said laminated structure to leave said single crystal
11 silicon channel layer suspended from said drain and source regions;
12 forming an oxide layer to cover said drain and source regions and said
13 single crystal silicon channel layer; and
14 forming a double-gate conductor over said oxide layer such that said
15 double-gate conductor includes a first conductor on a first side of said single
16 crystal silicon channel layer and a second conductor on a second side of said
17 single crystal silicon channel layer.

1 11. The method in claim 10, wherein, during said forming of said double-gate
2 conductor, said drain and source regions and said oxide layer self-align said
3 double-gate conductor.

1 12. The method in claim 10, wherein said forming of said laminated structure
2 includes forming a lower oxide layer adjacent one of said first insulating layers
3 and said method further comprises, after said forming of said double-gate
4 conductor, forming an upper oxide layer on an opposite side of said double-gate
5 conductor from said lower oxide layer, such that a thickness of said gate oxide
6 layer is independent of a thickness of said upper oxide layer and said lower oxide
7 layer.

1 13. The method in claim 10, wherein said forming of said drain and source
2 regions comprises epitaxially growing silicon in said openings from said single
3 crystal silicon channel layer.

1 14. The method in claim 13, wherein said epitaxially growing of said silicon
2 includes introducing one or more of Si, Ge, C, N and an alloy.

1 15. The method in claim 10, wherein said forming of said drain and source
2 regions comprises epitaxially growing silicon in a portion of said openings from
3 said single crystal silicon channel layer and filling a remainder of said openings
4 with amorphous silicon to complete said drain and source regions.

1 16. The method in claim 10, wherein:
2 said forming of said laminated structure includes attaching a silicon
3 substrate to said laminated structure;
4 said forming of said openings includes exposing said silicon substrate; and
5 said forming of said drain and source regions comprises epitaxially
6 growing silicon in said openings from said single crystal silicon channel layer and
7 said silicon substrate.

1 17. The method in claim 10, wherein, before said forming of said drain and

2 source regions, said method further comprises forming spacers in said openings.

1 18. A double-gate integrated circuit comprising:

2 a channel layer;

3 doped drain and source regions connected to said channel layer;

4 a gate insulating layer covering said channel layer and said doped drain

5 and source regions;

6 a double-gate conductor over said insulating layer, said double-gate

7 conductor including a first conductor on a first side of said channel layer and a

8 second conductor on a second side of said channel layer;

9 an upper insulator layer adjacent on a first side of said double-gate

10 conductor; and

11 a lower insulator layer on an opposite side of said double-gate conductor

12 from said upper insulator layer, wherein a thickness of said gate insulating layer is

13 independent of a thickness of said upper insulator layer and said lower insulator

14 layer.

1 19. The double-gate integrated circuit in claim 18, wherein, said first

2 conductor and said second conductor are self-aligned by said doped regions and

3 said gate insulating layer.

1 20. The double-gate integrated circuit in claim 18, wherein said doped drain

2 and source regions comprise silicon epitaxially grown from said channel layer.

1 21. The double-gate integrated circuit in claim 20, wherein said epitaxially
2 grown silicon includes one or more of Si, Ge, C, N and an alloy.

1 22. The double-gate integrated circuit in claim 18, wherein said drain and
2 source regions comprise amorphous silicon and silicon epitaxially grown from
3 said channel layer.

1 23. The double-gate integrated circuit in claim 18, further comprising a
2 substrate connected to said lower insulator layer, wherein said drain and source
3 regions comprise silicon epitaxially grown from said channel layer and from said
4 substrate.

1 24. The double-gate integrated circuit in claim 18, wherein said channel layer
2 comprises a single crystal silicon layer.